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Report on trade-off metrics for (self-) adaptive compensation and optimization techniques

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Authors:

| CEA          | Edith Beigne, Ivan Miro-Panades |

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# Table of contents

1. INTRODUCTION ................................................................. 3

2. LAVFS ARCHITECTURE USING VDD-HOPPING TECHNIQUE - REMINDER ...................................................... 3
   2.1. LOCAL DYNAMIC VOLTAGE SCALING AND VDD-HOPPING ......................................................................... 3
   2.2. GENERAL ARCHITECTURE .................................................................................................................. 4

3. LEAKAGE POWER COMPARED TO DYNAMIC POWER ......................................................................................... 4
   3.1. LEAKAGE POWER CONTRIBUTION .......................................................................................................... 5
   3.2. POWER RESULTS ACCORDING TO VOLTAGE VARIATIONS ......................................................................... 6
   3.3. POWER RESULTS ACCORDING TO TEMPERATURE VARIATIONS .................................................................. 6
   3.4. POWER RESULTS ACCORDING TO TEMPERATURE AND VOLTAGE VARIATIONS .............................................. 6

4. ENERGY GAINS COMPARED TO CLASSICAL APPROACHES ......................................................... ERROR! BOOKMARK NOT DEFINED.

5. CONCLUSION ................................................................................................................................. 7
1. Introduction

In this task, CEA has proposed a fine-grain Adaptive Voltage and Frequency Scaling (AVS) architecture to optimize energy efficiency in the presence of in-die variability. In section 2, a reminder is given for the proposed architecture that has been implemented in the project and particularly in WP5 for demonstration. The aim of this architecture is to save power during computation at fine-grain according to PVT variations and global applicative constraints.

Two processing elements in the MPSoC cluster have been instrumented with the proposed technique. The objective of this deliverable is to give an overview of power metrics and energy gain while using this architecture. All the results have been extracted form back-annotated simulations of the whole architecture at different operating point. The total dynamic and leakage power consumption will be taken into account. The proposed AVFS mechanism is finally compared to existing techniques: frequency scaling, classical DVFS without adaptation and ideal theoretical AVFS approach.

2. LAVFS architecture using Vdd-hopping technique - Reminder

For each System-on-Chip power domain, `Vdd-Hopping` is used: a technique as efficient as DC/DC power converters but much easier to integrate at chip level. Unlike previous AVS schemes, the functional core frequencies are adjusted regarding to local variability while the hopping ratio is determined to achieve a performance target. In this deliverable, we detail the proposed Local AVS architecture based on GALS. CEA propose a LAVS (Local Adaptive Voltage Scaling) architecture by adding adaptive capabilities to a previously developed LDVS (Local Dynamic Voltage Scaling) architecture [7]. The main objective is to maximize energy efficiency while respecting performance constraints. Because the LDVS architecture is based on a method called Vdd-Hopping with dithering, the usual AVS paradigm (frequency fixed by the application, supply voltage adjusted by a closed-loop control) had to be reversed. In our proposal, supply voltages are fixed, while two frequencies and the dithering ratio are adjusted using adaptive techniques. In this work, we have proposed a LAVS (Local Adaptive Voltage Scaling) architecture by adding adaptive capabilities to a previously developed LDVS (Local Dynamic Voltage Scaling) architecture [7]. The main objective is to maximize energy efficiency while respecting performance constraints. Because the LDVS architecture is based on a method called Vdd-Hopping with dithering, the usual AVS paradigm (frequency fixed by the application, supply voltage adjusted by a closed-loop control) had to be reversed. In our proposal, supply voltages are fixed, while two frequencies and the dithering ratio are adjusted using adaptive techniques.

2.1. Local Dynamic Voltage Scaling and Vdd-Hopping

To perform fine-grain voltage scaling on SoC and MPSoC containing more than ten functional cores, traditional DC/DC converters have reach their limit. The simplest ones are linear converters, small and easily integrated, but their efficiency decreases as the Vout/Vin ratio. More efficient converters like capacitive or inductive ones are widely used in the industry, but they are using capacitors and inductors that cannot be easily integrated. For multiple voltage converters one can either use dozens of external passives (taking lots of pads and board area, increasing board assembly time), integrate passives in standard silicon technologies (nearly doubling the chip area) or use special technologies like above IC integration (adding process steps, resulting in inductors with low quality factor).
2.2. General Architecture

In a system where Vdd-Hopping is used, there is no voltage to adjust, so we chose to adjust both the Fhigh and Flow frequencies. And because those frequencies are changed dynamically, the dithering ratio spent in the ‘high’ mode and the ‘low’ mode must also be adjusted in order to reach the target average frequency Ftarget. This architecture is called Local AVS because the frequencies are independently adjusted in every voltage/frequency domain depending on local variability factors. Except from performance targets, there should be no timing constraints between clocks on different domains, meaning the system should be GALS (Globally Asynchronous Locally Synchronous). The performance targets are set by the GPM (Global Power Manager) whose task is to find the right set of local constraints to optimize the whole chip power efficiency [16, 17].

The main elements of this architecture at the ‘functional core’ level are: the adaptation controller, whose task is to make sure that the functional core will be able to run at Fhigh (respectively Flow) when the Vhigh (respectively Vlow) power supply is selected and the performance controller, whose task is to make sure the performance target will be reached. As seen in 5, except for the additional adaptation controller and the Hardware Performance Monitors (HPM), this LAVS architecture share many common elements with a LDVS architecture.

The operating principle is the following:
- Using measurements made by HPMs, the adaptation controller make two safe estimates FmaxEstHigh and FmaxEstLow of the maximum frequency limit Fmax of the functional core when supplied by the Vhigh and Vlow sources.
- The two clock generators generate low-jitter clock signals at the selected frequencies.
- Using a reference clock Fref the performance controller measures the frequencies actually generated and calculate the optimal ‘high/low’ dithering duty ratio of the hopping sequence.
- Finally, the PSS, the clock selector and the sequencer are used to make safe transitions (transitions with no delay fault in the functional core) between ‘high’ and ‘low’ power modes.

More details on each device will be given in next section.

3. Leakage power compared to dynamic power
3.1. Leakage power contribution

Leakage power proportion has been simulated compared to total dynamic power on two processors of the architecture PE0 (Processing Element number 0) and PE2 (processing Element number 2). Leakage proportion is quite low due to high k metal gate used in this 32 nm STMicroelectronics technology. Globally at 500MHz, mainly dynamic power consumption will be considered. Reducing Vdd will efficiently reduce both Leakage and dynamic power.
3.2. **Power results according to voltage variations**

As far as dynamic voltage scaling is considered, we have simulated the power consumption with respect to voltage supply variations. It shows that leakage power increases quadratically at higher voltages.

3.3. **Power results according to temperature variations**

The architecture is adaptive to Process-Voltage-Temperature variations, and a processor behavior with respect to temperature variations have to be validated. It clearly shows that leakage power is still an issue while temperature is increasing. Activity or voltage have to be reduced as temperature increase will lead to leakage increase and leakage increase will lead to temperature increase.

3.4. **Power results according to temperature and voltage variations**
Both temperature and voltage variations are represented on this 3D graph showing that a trade-off can be found between a high performance block in terms of speed and power in all the power modes proposed in the architecture. V/F optimum point will be found considering this trade-off.

4. Conclusion

The proposed fine-grain adaptive DVFS architecture allows high gains in terms of energy and frequency compared to classic worst-case or DVFS approaches. In other words, using three fixed voltage supplies, the circuit is able to dynamically reach an optimal frequency/energy point depending on intrinsic PVT variations and applicative constraints for a low area overhead.